TPS60111
REGULATED 5-V 150-mA LOW-NOISE CHARGE PUMP DC/DC CONVERTER
SLVS216 – JUNE 1999

features
- Up to 150-mA Output Current
- Less Than 10-mVpp Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 5-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 2.7-V to 5.4-V Input Voltage Range
- 60-µA Quiescent Supply Current
- 0.05-µA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package

applications
- Replaces DC/DC Converters With Inductors in
  - Battery-Powered Applications
  - Li-Ion Battery to 5-V Conversion
  - Portable Instruments
  - Battery-Powered Microprocessor Systems
  - Miniature Equipment
  - Backup-Battery Boost Converters
  - PDAs
  - Laptops
  - Handheld Instrumentation
  - Medical Instruments

description
The TPS60111 step-up, regulated charge pump generates a 5-V ±4% output voltage from a 2.7-V to 5.4-V input voltage (three alkaline, NiCd, or NiMH batteries; or, one lithium or lithium ion battery). Output current is 150 mA from a 3-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 3-V input, the TPS60111 can start into full load with loads as low as 33 Ω.

The TPS60111 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60111 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-µA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc/dc converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

output voltage ripple

<table>
<thead>
<tr>
<th>V0 - Output Voltage - V</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.2</td>
</tr>
<tr>
<td>5.15</td>
</tr>
<tr>
<td>5.1</td>
</tr>
<tr>
<td>5.05</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>4.95</td>
</tr>
<tr>
<td>4.9</td>
</tr>
<tr>
<td>4.85</td>
</tr>
<tr>
<td>4.8</td>
</tr>
</tbody>
</table>

V0 = Output Voltage - V

Figure 1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.
Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

Available Options

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>TSSOP (PWP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVAILABLE OPTIONS</td>
<td></td>
</tr>
<tr>
<td>20-pin TSSOP PowerPAD package</td>
<td></td>
</tr>
</tbody>
</table>

Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>Terminal No.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>19</td>
<td>I</td>
<td>Input for external clock signal. If the internal clock is used, connect this terminal to GND.</td>
</tr>
<tr>
<td>C1+</td>
<td>6</td>
<td>I</td>
<td>Positive terminal of the charge-pump capacitor ( C_{1F} )</td>
</tr>
<tr>
<td>C1−</td>
<td>8</td>
<td>I</td>
<td>Negative terminal of the charge-pump capacitor ( C_{1F} )</td>
</tr>
<tr>
<td>C2+</td>
<td>15</td>
<td>I</td>
<td>Positive terminal of the charge-pump capacitor ( C_{2F} )</td>
</tr>
<tr>
<td>C2−</td>
<td>13</td>
<td>I</td>
<td>Negative terminal of the charge-pump capacitor ( C_{2F} )</td>
</tr>
<tr>
<td>COM</td>
<td>18</td>
<td>I</td>
<td>Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor.</td>
</tr>
<tr>
<td>ENABLE</td>
<td>3</td>
<td>I</td>
<td>ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 ( \mu )A when ENABLE is a logic low. Connect ENABLE to IN for normal operation.</td>
</tr>
<tr>
<td>FB</td>
<td>4</td>
<td>I</td>
<td>FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on-chip to match internal reference voltage of 1.22 V.</td>
</tr>
<tr>
<td>GND</td>
<td>1, 20</td>
<td>I</td>
<td>GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.</td>
</tr>
<tr>
<td>IN</td>
<td>7, 14</td>
<td>I</td>
<td>Supply Input. Connect to an input supply in the 2.7-V to 5.4-V range. Bypass IN to GND with a ( (C_{O}/2) ) ( \mu )F capacitor. Connect both INs through a short trace.</td>
</tr>
<tr>
<td>OUT</td>
<td>5, 16</td>
<td>O</td>
<td>Regulated 5-V power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor ( C_{O} ).</td>
</tr>
<tr>
<td>PGND</td>
<td>9–12</td>
<td></td>
<td>PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together.</td>
</tr>
<tr>
<td>SKIP</td>
<td>17</td>
<td>I</td>
<td>Mode selection. When SKIP is logic low the charge pump operates in constant-frequency mode. Thus output ripple and noise are minimized. When SKIP is connected to IN, the regulator operates in low-quesient-current pulse-skip mode.</td>
</tr>
<tr>
<td>SYNC</td>
<td>2</td>
<td>I</td>
<td>Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through CLK.</td>
</tr>
</tbody>
</table>
absolute maximum ratings (unless otherwise noted)†‡

Input voltage range, $V_I$ (IN, OUT, ENABLE, SKIP, COM, CLK, FB, SYNC) ................. $-0.3 \text{ V to } 5.5 \text{ V}$
Differential input voltage, $V_{ID}$ (C1+, C2+ to GND) ........................................ $-0.3 \text{ V to } (V_O + 0.3 \text{ V})$
Differential input voltage, $V_{ID}$ (C1–, C2– to GND) ........................................ $-0.3 \text{ V to } (V_{IN} + 0.3 \text{ V})$
Continuous total power dissipation ................................................................. See Dissipation Rating Tables
Continuous output current ............................................................. 200 mA
Storage temperature range, $T_{stg}$ .............................................................. $-55^\circ C \text{ to } 150^\circ C$
Lead temperature 1.6 mm (1/16 inch) from case for 10s ........................................ 260°C
Maximum junction temperature, $T_J$ ........................................................... 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ $V_{ENABLE}$, $V_{SKIP}$, $V_{COM}$, $V_{CLK}$ and $V_{SYNC}$ can exceed $V_{IN}$ up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.
electrical characteristics at $C_{IN} = 15 \, \mu F$, $C_{F1} = C_{F2} = 2.2 \, \mu F$, $C_{O} = 33 \, \mu F$, $T_{C} = -40^\circ C$ to $85^\circ C$, $V_{IN} = 3V$, $V_{FB} = V_{O}$, $V_{ENABLE} = V_{IN}$, $V_{SKIP} = V_{IN}$ or $0$ V and $V_{COM} = V_{CLK} = V_{SYNC} = 0$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage</td>
<td>2.7</td>
<td>5.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{O(MAX)}$</td>
<td>Maximum output current</td>
<td>150</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{O}$</td>
<td>Output voltage</td>
<td>$2.7 &lt; V_{IN} &lt; 3$ V, $0 &lt; I_{O} &lt; 75$ mA, $T_C = 25^\circ C$</td>
<td>4.8</td>
<td>5</td>
<td>5.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$3 &lt; V_{IN} &lt; 5$ V, $0 &lt; I_{O} &lt; 150$ mA</td>
<td>4.8</td>
<td>5</td>
<td>5.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$5 &lt; V_{IN} &lt; 5.4$ V, $0 &lt; I_{O} &lt; 150$ mA</td>
<td>4.8</td>
<td>5</td>
<td>5.25</td>
</tr>
<tr>
<td>$V_{O(RIP)}$</td>
<td>Output voltage ripple</td>
<td>$I_{O} = 150$ mA, $V_{SKIP} = 0$ V</td>
<td>10†</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{O(LEAK)}$</td>
<td>Output leakage current</td>
<td>$V_{IN} = 3.6$ V, $V_{ENABLE} = 0$ V</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{Q}$</td>
<td>Quiescent current (no-load input current)</td>
<td>$V_{SKIP} = V_{IN} = 3.6$ V, $V_{IN} = 3.6$ V</td>
<td>60</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>$I_{DD(SDN)}$</td>
<td>Shutdown supply current</td>
<td>$V_{IN} = 3.6$ V, $V_{ENABLE} = 0$ V</td>
<td>0.05</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$f_{OSC(int)}$</td>
<td>Internal switching frequency</td>
<td>$V_{IN} = 3.6$ V</td>
<td>200</td>
<td>300</td>
<td>400</td>
</tr>
<tr>
<td>$f_{OSC(ext)}$</td>
<td>External clock frequency</td>
<td>$V_{SYNC} = V_{IN}$, $V_{IN} = 2.7$ V to 5.4 V</td>
<td>400</td>
<td>600</td>
<td>800</td>
</tr>
<tr>
<td></td>
<td>External clock duty cycle</td>
<td>$V_{SYNC} = V_{IN}$, $V_{IN} = 2.7$ V to 5.4 V</td>
<td>20%</td>
<td></td>
<td>80%</td>
</tr>
<tr>
<td></td>
<td>Efficiency</td>
<td>$I_{O} = 75$ mA</td>
<td>80%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{INL}$</td>
<td>Input voltage low, $ENABLE$, $SKIP$, $COM$, $CLK$, $SYNC$</td>
<td>$V_{IN} = 2.7$ V</td>
<td>0.3 ×</td>
<td>$V_{IN}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{INH}$</td>
<td>Input voltage high, $ENABLE$, $SKIP$, $COM$, $CLK$, $SYNC$</td>
<td>$V_{IN} = 5.4$ V</td>
<td>0.7 ×</td>
<td>$V_{IN}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{II(LEAK)}$</td>
<td>Input leakage current, $ENABLE$, $SKIP$, $COM$, $CLK$, $SYNC$</td>
<td>$V_{ENABLE} = V_{SKIP} = V_{COM} = V_{CLK} = V_{SYNC} = V_{GND}$ or $V_{IN}$</td>
<td>0.01</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output load regulation</td>
<td>$V_{O} = 5$ V, $T_C = 25^\circ C$</td>
<td>1 mA &lt; $I_{O} &lt; 150$ mA</td>
<td>0.002</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output line regulation</td>
<td>$3 &lt; V_{IN} &lt; 5$ V, $I_{O} = 75$ mA, $T_C = 25^\circ C$</td>
<td>$V_{O} = 5$ V, $V_{O} = 0$ V</td>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Short circuit current</td>
<td>$V_{IN} = 3.6$ V, $T_C = 25^\circ C$</td>
<td>$V_{O} = 0$ V</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.
‡ Achieved with $C_{O} = 22 \, \mu F + 10 \, \mu F$ X5R dielectric ceramic capacitor
TYPICAL CHARACTERISTICS†

EFFICIENCY vs OUTPUT CURRENT

Figure 5

EFFICIENCY vs OUTPUT CURRENT

Figure 6

QUIESCENT SUPPLY CURRENT vs INPUT VOLTAGE

Figure 7

QUIESCENT SUPPLY CURRENT vs INPUT VOLTAGE

Figure 8

†TC = 25°C, VCOM = VSYNC = 0 V, Cin = 15 μF, CF1 and CF2 = 2.2 μF (X7R ceramic), CO = 33 μF, unless otherwise noted
TYPICAL CHARACTERISTICS†

Figure 9

OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 10

OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 11

OUTPUT VOLTAGE vs INPUT VOLTAGE

Figure 12

OUTPUT VOLTAGE vs INPUT VOLTAGE

†TC = 25°C, VCOM = VSYNC = 0 V, CIN = 15 µF, CF1 and CF2 = 2.2 µF (X7R ceramic), CO = 33 µF, unless otherwise noted
TYPICAL CHARACTERISTICS†

**OUTPUT VOLTAGE vs TIME**

- **Figure 13**
  - $V_{\text{SKIP}} = 0 \text{ V}$
  - $V_{\text{IN}} = 3.6 \text{ V}$
  - $I_O = 150 \text{ mA}$
  - $C_O = 22 \mu\text{F} + 10 \mu\text{F}$ X5R ceramic

**OUTPUT VOLTAGE vs TIME**

- **Figure 14**
  - $V_{\text{SKIP}} = V_{\text{IN}}$
  - $V_{\text{IN}} = 3.6 \text{ V}$
  - $I_O = 150 \text{ mA}$

**LOAD TRANSIENT RESPONSE**

- **Figure 15**
  - $V_{\text{SKIP}} = 0 \text{ V}$
  - $I_O = 10 \text{ mA}$ to $150 \text{ mA}$
  - $V_{\text{IN}} = 3.6 \text{ V}$

**LOAD TRANSIENT RESPONSE**

- **Figure 16**
  - $V_{\text{SKIP}} = V_{\text{IN}} = 3.6 \text{ V}$
  - $I_O = 10 \text{ mA}$ to $150 \text{ mA}$
  - Pulse-Skip Mode

†$T_C = 25^\circ\text{C}$, $V_{\text{COM}} = V_{\text{SYNC}} = 0 \text{ V}$, $C_{\text{IN}} = 15 \mu\text{F}$, $C_{\text{F1}}$ and $C_{\text{F2}} = 2.2 \mu\text{F}$ (X7R ceramic), $C_O = 33 \mu\text{F}$, unless otherwise noted
**Typical Characteristics†**

**Line Transient Response**

- **Figure 17**
  - Output Voltage: \(V_O\)
  - Input Voltage: \(V_IN\)
  - \(V_{\text{SKIP}} = 0\) V
  - \(I_O = 150\) mA
  - Constant Frequency Mode

- **Figure 18**
  - Output Voltage: \(V_O\)
  - Input Voltage: \(V_IN\)
  - \(V_{\text{SKIP}} = V_IN\)
  - \(I_O = 150\) mA
  - Pulse-Skip Mode

**Frequency Spectrum**

- **Figure 19**
  - Output – dB, V
  - \(V_{\text{SKIP}} = 0\) V
  - \(V_IN = 3\) V
  - \(I_O = 150\) mA
  - \(RBW = 300\) Hz
  - Constant Frequency Mode

- **Figure 20**
  - Output – dB, V
  - \(V_{\text{SKIP}} = V_IN\)
  - \(V_IN = 3\) V
  - \(I_O = 150\) mA
  - \(RBW = 300\) Hz
  - Pulse-Skip Mode

†TC = 25°C, \(V_{\text{COM}} = V_{\text{SYNC}} = 0\) V, \(C_{\text{IN}} = 15\) µF, \(C_{F1}\) and \(C_{F2} = 2.2\) µF (X7R ceramic), \(C_O = 33\) µF, unless otherwise noted

‡Test circuit: TPS60110EVM–132 with TPS60111
TPS60111
REGULATED 5-V 150-mA LOW-NOISE
CHARGE PUMP DC/DC CONVERTER
SLVS216 – JUNE 1999

TYPICAL CHARACTERISTICS†

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

\[
\begin{align*}
V_{\text{SKIP}} &= 0 \text{ V} \\
V_{\text{IN}} &= 3 \text{ V} \\
I_O &= 10 \text{ mA} \\
\text{RBW} &= 300 \text{ Hz}
\end{align*}
\]

Output – dB V

f – Frequency – MHz

Figure 21

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

\[
\begin{align*}
V_{\text{SKIP}} &= V_{\text{IN}} \\
V_{\text{IN}} &= 3 \text{ V} \\
I_O &= 10 \text{ mA} \\
\text{RBW} &= 300 \text{ Hz}
\end{align*}
\]

Output – dB V

f – Frequency – MHz

Figure 22

EFFICIENCY
VS
INPUT VOLTAGE

\[
I_O = 150 \text{ mA}
\]

Efficiency – %

\[
\begin{align*}
\text{Skip} &= \text{High} \\
\text{Skip} &= \text{Low}
\end{align*}
\]

\[
\begin{align*}
V_{\text{IN}} &= \text{Input Voltage – V} \\
I_O &= 150 \text{ mA}
\end{align*}
\]

Figure 23

START-UP TIMING

\[
R_0 = 33.3 \Omega \\
V_{\text{IN}} = 3 \text{ V}
\]

\[
\begin{align*}
V_O = \text{Output Voltage – V} \\
\text{Enable} \\
\text{OUTPUT}
\end{align*}
\]

\[
\begin{align*}
\text{t} &= \text{Time – \mu s} \\
\text{t} &= 0, 200, 400, 600, 800, 1000, 1200
\end{align*}
\]

Figure 24

†\(T_C = 25^\circ\text{C}, V_{\text{COM}} = V_{\text{SYNC}} = 0 \text{ V}, C_{\text{IN}} = 15 \mu\text{F}, C_{F1} \text{ and } C_{F2} = 2.2 \mu\text{F (X7R ceramic)}, C_O = 33 \mu\text{F}, \) unless otherwise noted

‡Test circuit: TPS60110EVM–132 with TPS60111
The TPS60111 charge pump provides a regulated 5-V output from a 2.7-V to 5.4-V input. It delivers a maximum load current of 150 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60111 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 25).

Figure 25. Functional Block Diagram TPS60111

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (CxF) in one half of the period. During the other half of the period (transfer phase), CxF is placed in series with the input to transfer its charge to CO. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 5 V, the TPS60111 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.
detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage $V_O$ reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP and COM. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 5 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 5 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 5 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60111 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency $f_{OSC}$. The control circuit, fed from the error amplifier, controls the charge on $C_{1F}$ and $C_{2F}$ by driving the gates of the FETs $T_{12}/T_{13}$ and $T_{22}/T_{23}$, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across $C_{1F}$ and $C_{2F}$. This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

![Typical Operating Circuit TPS60111 in Constant Frequency Mode](image)

**Figure 26. Typical Operating Circuit TPS60111 in Constant Frequency Mode**

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>PULSE-SKIP MODE (SKIP = High)</th>
<th>CONSTANT-FREQUENCY MODE (SKIP = Low)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Best light-load efficiency</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Smallest external component size for a given output ripple</td>
<td>Small amplitude</td>
<td>Very small amplitude</td>
</tr>
<tr>
<td>Output ripple amplitude</td>
<td>Variable</td>
<td>Constant</td>
</tr>
<tr>
<td>Output ripple frequency</td>
<td>Very good</td>
<td>Good</td>
</tr>
</tbody>
</table>

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.
push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (CxF) in one-half of the period. During the other half of the period (transfer phase), CxF is placed in series with the input to transfer its charge to CO. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60111 in push-pull mode is shown in Figure 1 and Figure 26.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (CF) in one half of the period. During the other half of the period (transfer phase), CF is placed in series with the input to transfer its charge to CO. In single-ended operating mode only one transfer capacitor (CF = C1F + C2F) is required, resulting in less board space.

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**Figure 27. Typical Operating Circuit TPS60111 in Single-Ended Operating Mode**

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>PUSH-PULL MODE (COM = Low)</th>
<th>SINGLE-ENDED MODE (COM = High)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output ripple amplitude</td>
<td>Small amplitude</td>
<td>Large amplitude</td>
</tr>
<tr>
<td>Smallest board space</td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>
detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05-µA (1-µA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 µA max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 20 µs. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device operates at a user-defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive CLK. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

![Figure 28. Typical Operating Circuit TPS60111 with External Synchronization](image)
APPLICATION INFORMATION

capacitor selection

The TPS60111 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_x) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_IN is recommended to be about two to four times as large as C_x.

The output capacitor (C_O) can be selected from 8-times to 50-times larger than C_x, depending on the mode of operation and ripple tolerance†. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation† (pulse-skip mode)

<table>
<thead>
<tr>
<th>V_IN [V]</th>
<th>I_O [mA]</th>
<th>C_IN [µF]</th>
<th>C_x [µF]</th>
<th>C_O [µF]</th>
<th>OUTPUT VOLTAGE RIPPLE V_PPP [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TANTALUM</td>
<td>CERAMIC</td>
<td>TANTALUM</td>
<td>CERAMIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.6</td>
<td>75</td>
<td>4.7</td>
<td>1</td>
<td>15</td>
<td>150</td>
</tr>
<tr>
<td>3.6</td>
<td>75</td>
<td>4.7 (X7R)</td>
<td>1</td>
<td>10 (X5R)</td>
<td>105</td>
</tr>
<tr>
<td>3.6</td>
<td>150</td>
<td>4.7</td>
<td>1</td>
<td>15</td>
<td>150</td>
</tr>
<tr>
<td>3.6</td>
<td>150</td>
<td>4.7 (X7R)</td>
<td>1</td>
<td>10 (X5R)</td>
<td>105</td>
</tr>
</tbody>
</table>

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation† (constant-frequency mode)

<table>
<thead>
<tr>
<th>V_IN [V]</th>
<th>I_O [mA]</th>
<th>C_IN [µF]</th>
<th>C_x [µF]</th>
<th>C_O [µF]</th>
<th>OUTPUT VOLTAGE RIPPLE V_PPP [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TANTALUM</td>
<td>CERAMIC</td>
<td>TANTALUM</td>
<td>CERAMIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.6</td>
<td>75</td>
<td>4.7</td>
<td>1</td>
<td>33</td>
<td>10</td>
</tr>
<tr>
<td>3.6</td>
<td>75</td>
<td>4.7 (X7R)</td>
<td>1</td>
<td>22 + 10 (X5R)</td>
<td>6</td>
</tr>
<tr>
<td>3.6</td>
<td>150</td>
<td>4.7</td>
<td>1</td>
<td>33</td>
<td>17</td>
</tr>
<tr>
<td>3.6</td>
<td>150</td>
<td>4.7 (X7R)</td>
<td>1</td>
<td>22 + 10 (X5R)</td>
<td>10</td>
</tr>
</tbody>
</table>

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

† In constant-frequency mode always select C_O ≥ 33 µF
APPLICATION INFORMATION

For the TPS60111, the smallest board space size can be achieved using Sprague’s 595D–series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might soon become competitive in size.

Table 5. Recommended Capacitors

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
<th>CAPACITANCE</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Taiyo Yuden</td>
<td>LMK212BJ105KG–T</td>
<td>1 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td></td>
<td>LMK212BJ225MG–T</td>
<td>2.2 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td></td>
<td>LMK316BJ475KL–T</td>
<td>4.7 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td></td>
<td>JMK316BJ106ML–T</td>
<td>10 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td></td>
<td>LMK432BJ226MM–T</td>
<td>22 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td>AVX</td>
<td>0805ZC105KAT2A</td>
<td>1 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td></td>
<td>1206ZC225KAT2A</td>
<td>2.2 µF</td>
<td>Ceramic</td>
</tr>
<tr>
<td></td>
<td>TPSC475K035R0600</td>
<td>4.7 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>TPSC156K020R0450</td>
<td>15 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>TPSC336K010R0375</td>
<td>33 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td>Sprague</td>
<td>595D475X016A2T</td>
<td>4.7 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>595D156X063R32T</td>
<td>15 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>595D156X016B2T</td>
<td>15 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>595D336X063R32T</td>
<td>33 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>595D336X0016B2T</td>
<td>33 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>595D336X0016C2T</td>
<td>33 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td>Kemet</td>
<td>T494B475M010AS</td>
<td>4.7 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>T494C156K010AS</td>
<td>15 µF</td>
<td>Tantalum</td>
</tr>
<tr>
<td></td>
<td>T494C336K010AS</td>
<td>33 µF</td>
<td>Tantalum</td>
</tr>
</tbody>
</table>

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>CAPACITOR TYPE</th>
<th>INTERNET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Taiyo Yuden</td>
<td>X7R/X5R ceramic</td>
<td><a href="http://www.t%E2%80%93yuden.com">www.t–yuden.com</a></td>
</tr>
<tr>
<td></td>
<td>TPS–series tantalum</td>
<td></td>
</tr>
<tr>
<td>AVX</td>
<td>X7R/X5R ceramic</td>
<td><a href="http://www.avxcorp.com">www.avxcorp.com</a></td>
</tr>
<tr>
<td></td>
<td>TPS–series tantalum</td>
<td></td>
</tr>
<tr>
<td>Sprague</td>
<td>595D–series tantalum</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td></td>
<td>593D–series tantalum</td>
<td></td>
</tr>
<tr>
<td>Kemet</td>
<td>T494–series tantalum</td>
<td><a href="http://www.kemet.com">www.kemet.com</a></td>
</tr>
</tbody>
</table>

power dissipation

The power dissipated in the TPS60111 depends on output current and is approximated by:

\[ P_{\text{DISS}} = I_O \times (2 \times V_{\text{IN}} - V_O) \text{ for } I_O < < I_O \]

\( P_{\text{DISS}} \) must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.
APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 29. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achieve optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plain only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

Figure 29. Recommended PCB Layout for TPS60111 (top view)
applications proposals

TPS60111 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 30. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

Figure 30. TPS60111 with LC Filter for Ultra Low Output Ripple Applications

Additional information: PowerPAD application report (SLMA002)
MECHANICAL DATA

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20-PIN SHOWN

DEVICE MARKING: 

- PWP
- (R-PDSO-G**)

DIAGRAM

- 

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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